

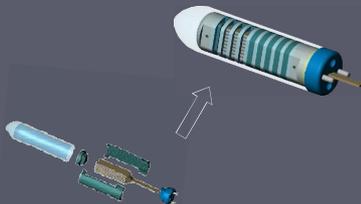
# Development and Test of Micro-Cables for Thin Silicon Detector Modules in a Prostate Probe.

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## Introduction

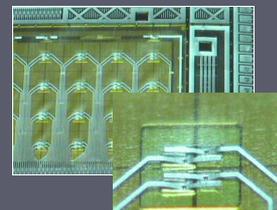
- Silicon probes can considerably improve the performance of imaging devices in Nuclear Medicine
- Diagnosis
  - ✓ Compton cameras
  - ✓ Compton prostate probe (shown in the picture) by improving both the sensitivity (due to the near field operation) and the spatial resolution considerably (G. Llosa et. al. Nuc. Ins. Meth. A Vol 527, 58-61 (2004))
  - ✓ PET magnifying glasses to provide enhanced resolution in regions of interest
- Therapy
  - ✓ An add-on to a conventional InBeam PET for light ion and proton therapy which would increase the sensitivity by detecting prompt gammas when operating the PET and the probe on Compton camera mode



- The silicon probes are built as densely packed stacks of silicon pad sensors and packaging is a very important issue
- TAB (Tape Automated Bonding) is a possible technology that we are exploring
- Both silicon sensors and their readout chips VATAGP3 from IDEAS<sup>1</sup> have been TABed to their corresponding cables and measured

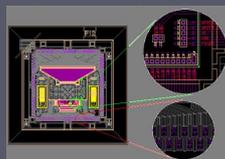
## Micro-Cable Technology

- The micro-cable technology was developed by SRTIIM for use in space electronics.
- It connects (via ultrasounds) the pads of a device (ASIC, silicon detector) to aluminium printed traces on the micro-cable.
- The micro-cable on a flex support (Kapton) carries signals between pads of two different devices.
- Bonding windows etched through the Kapton to allow for pressing the Al traces through and bond them directly to the pads beneath.
- Typically
  - ✓ minimum pitch ~100 μm
  - ✓ thickness: Al 14 μm, Kapton 12 μm
  - ✓ bus assemblies (up to 10 layers)
- Similar to standard TAB technology
  - ✓ it is bump-less
  - ✓ very thin
  - ✓ bond force required is small (10-15 grams)



- Elegant solution for
  - ✓ flexible and compact interconnection between ASICs and sensors
  - ✓ stacking silicon sensors to form a detection volume filled with more than 90% of active detector.
- The use of a polyimide layer of 70 micron thickness was essential to reduce the load capacitance of the traces at the input of the amplifier to acceptable values.

## Setup of the ASIC module



- A chip cable was TABed to VATA3 readout chips with 128 channels. This chip has already been used in prototype Compton probes to readout the signal of the silicon pad sensors.
- The chip cable was tested using a standard socket IC51-4364 (Yamaichi, Japan).

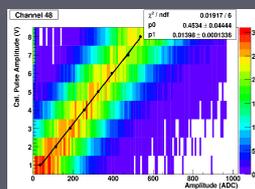
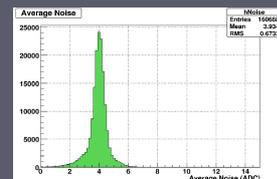
- TABed chips were mounted on a supporting frame, as shown on the picture below. The frame was in turn mounted on a clamp which was mounted on an intermediate board and the latter connected to the DAQ board in charge of generating the readout sequences.



## Results of the ASIC module

To check the functionality of the front-end ASIC we used a calibration pulse which was generated by an external pulse generator and injected on the calibration pad of the chip.

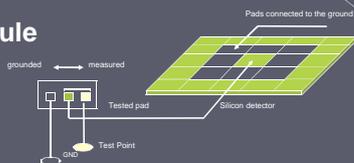
➤ The chip response versus the test pulse amplitude is shown in the "gain curve" (figure below)



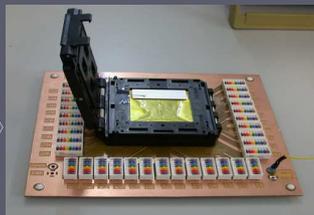
- The figure above shows the average value of the noise after common mode subtraction in units of ADC.
- Wire bonded VATA3 chips exhibit a similar noise performance.
- This result, therefore, demonstrates that TAB technology does not introduce any performance penalty.

## Setup of the Detector Module

- Developed by SRTIM, Kharkov
- A silicon detector (46 mm long, 14 mm wide and 1 mm thick) was TABed and held in a supporting frame
- The frame was housed in a standard socket IC51 - 3244 (Yamaichi, Japan).
- The clamp was mounted on a custom designed board for the test of the detector cable
- Connecting one pad to the test point and all its neighbours to ground we measured the leakage current on that pad avoiding contributions from other pads.

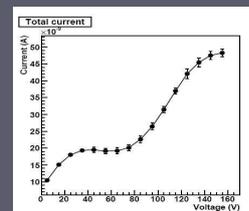
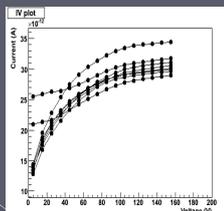
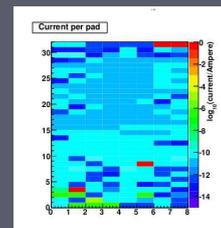


- Each switch connects one pad either to a test output or to ground (as shown in the figure above).
- This method allowed the test of the 256 pads separately.

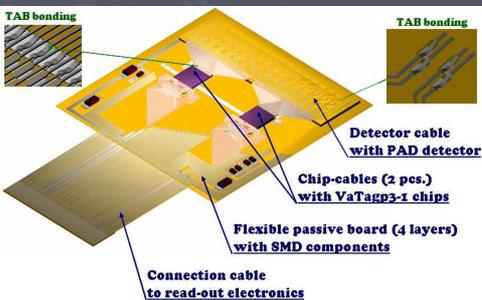


## Results of the Detector module

- The measured current on the test output as a function of the bias (setting all the pads to ground and only one to the test output) produced the IV curve shown in the figure below.
- The current measured per pad was ~34pA at 150V bias voltage.
- The measurements were made at room temperature.
- The figure on the right represents the leakage current measured on each pad of the detector.
- Most of the pads produce a leakage current of about 34pA at 150V
- The number of pads drawing currents compatible with zero represent a small percentage and are concentrated on the periphery so we believe that failure is due to handling and mechanical stresses after the TAB process.



- The left figure shows the current measured in the HV return line. It therefore represents the total leakage current of the detector.
- The step at 60V is due to the guard current becoming more important for higher voltages.
- The curves show that the detector gets fully depleted at 150V.
- The total current of 50nA is compatible with 50-100pA measured per each pad.



## Conclusions

- Silicon sensors and readout chips VATAGP3 from IDEAS<sup>1</sup> were TABed to their corresponding cables and tested successfully.
- A total of 256 interconnection pads from the silicon microstrip detector were connected to two readout chips.
- TAB does not deteriorate the electrical performance of the ASICs and we have proved that the yield of the connection of the detector pads is high (82%).
- Detector-cable and chip-cable assembly were TABed to a very thin PCB, being a Kapton cable soldered to the PCB for connection to the data acquisition system, achieving a total height of only 1.2 mm (shown on the right).
- The very high density packaging of silicon detector modules achieved is suitable to be employed in medical imaging modalities SPECT and PET.
- The use of micro cables gives the designers more possibilities like flexible, low mass and densely packed interconnections.
- TAB technology offers an elegant solution for a flexible and compact interconnection between the readout ASICs, the silicon sensor and the hybrid board.

