ALIBAVA TEST REPORT

The test of the system has been divided in different parts to validate the different parts of the motherboard hardware/firmware and the software. The following points explain the test activities carried out and their results.

1. Connection verification between the motherboard and the daughterboard.

A daughter board fully populated, but with the Beetle chips not connected, was used for this. The daughterboard and the daughterboard were connected with ribbon cable. Then the continuity and the agreement of each signal of the cable was checked. As a result, the IDC connector of the motherboard had to be changed of position (from top to the bottom of the motherboard) for obtaining the correct connections between the signals of the motherboard and the daughterboard.

2. Daughterboard power supply levels and fast control (LVDS) signals check.

The same daughterboard was used for this task. The motherboard and the daughterboard were connected with ribbon cable and the system was powered. The different power levels and LVDS signals were measured with a scope at the daughterboard. The signals and power levels were the expected and are shown in the following figures.

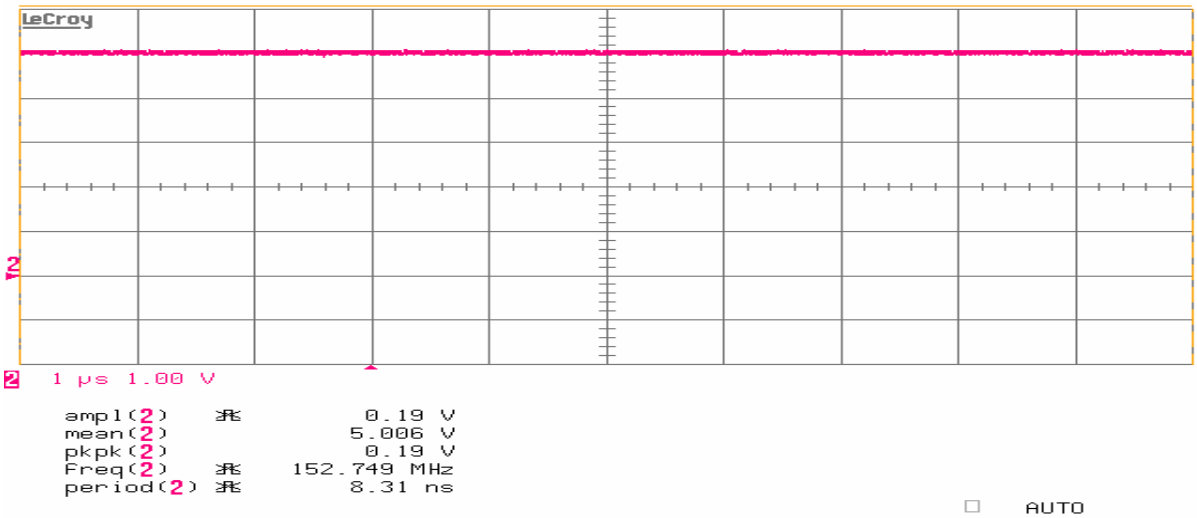

Figure 1. 5 V Power Supply.

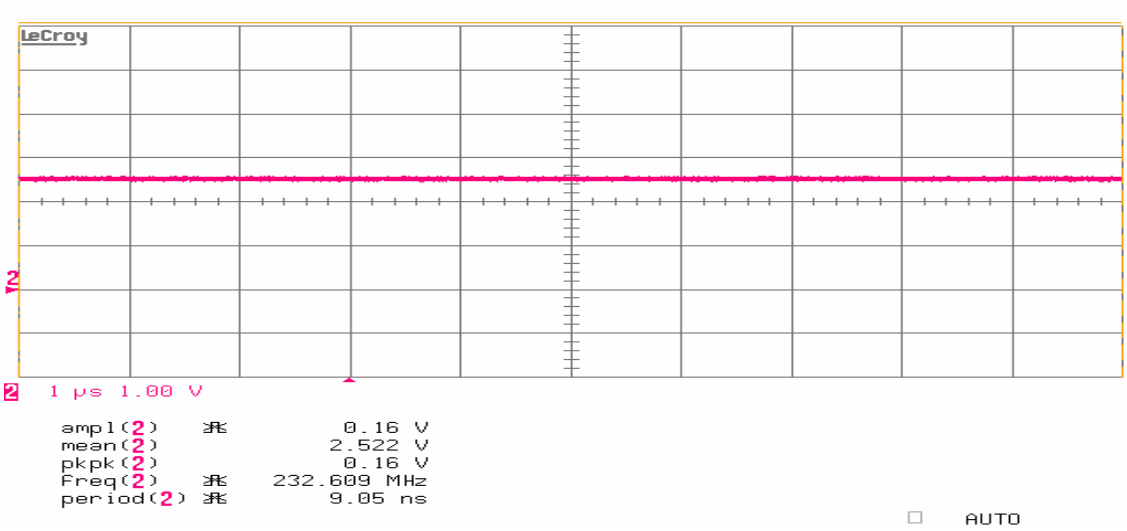

Figure 2. 2.5 V Power Supply 1.

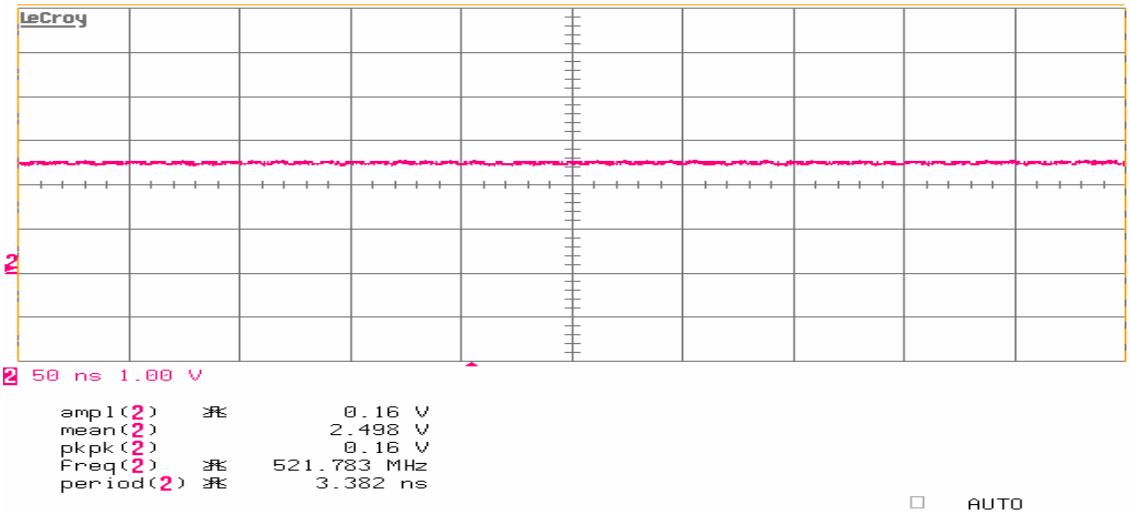

Figure 3. 2.5 V Power Supply 2.

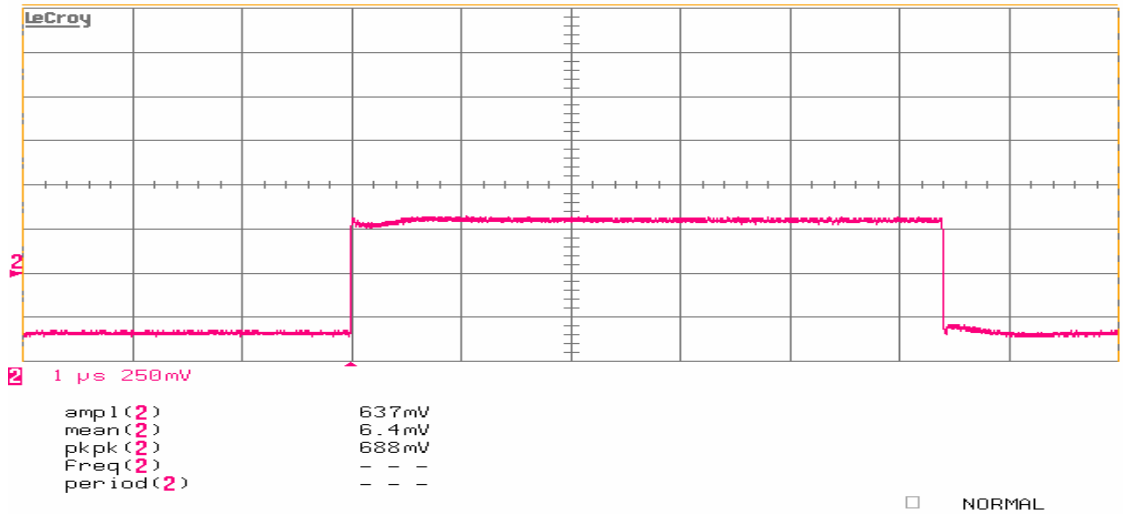

Figure 4. Beetle Reset Fast Control Signal (LVDS).

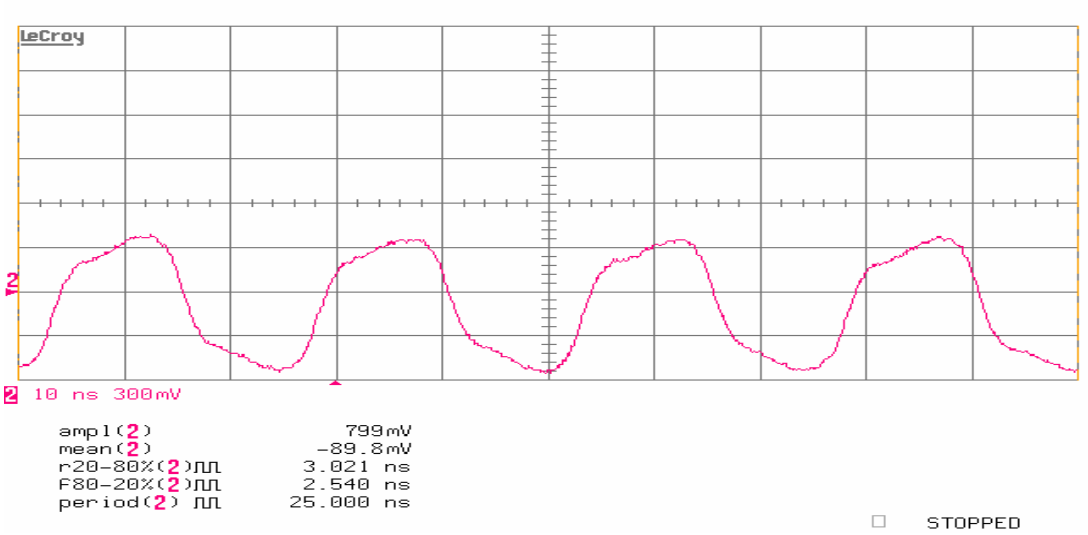

Figure 5. Beetle CLK Fast Control Signal (LVDS).

3. Beetle Configuration Test.

For this task a daughterboard fully populated with the Beetle chips connected was used. The motherboard and the daughterboard were connected with ribbon cable and the system was powered. The test was carried out firstly with Matlab for controlling the system and finally with the custom software developed by Carlos Lacasta. As a result, the Beetle chips were configured correctly.

The Beetle registers configured in this system during this state are the following; register 0 to register 5 with nominal values (Itp, Ipre, Isha, Ibuf, Vfp, Vfs), register 10 to register 15 with nominal values (Ipipe, Vd, Vdcl Ivoltbuf, Isf , Icurrbuf), register 16 fixed to 128 (Latency) and register 17 to register 19 for analog readout onto one port at 40 MHz (ROCtrl, RClkDiv, CompCtrl).

Once the registers are configured, the daughter board current consumption agrees with the specification of the daughterboard (450 mA aprox.). The following figure shows the SDA and SCL signals when configuring the Beetle chips.

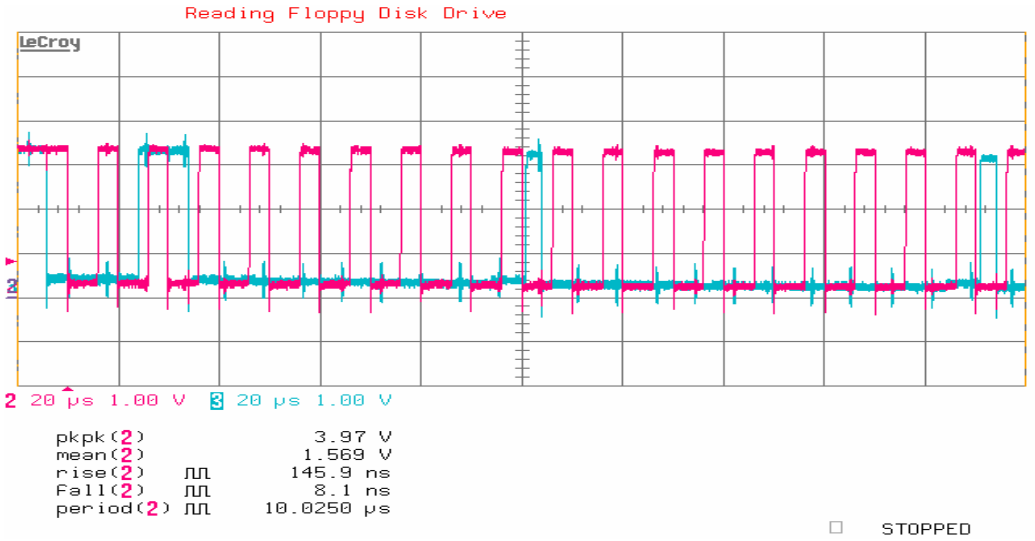

Figure 5. SDA and SCL signals when configuring the Beetle chips (SCL signal number 2 and SDA signal number 3).

4. Calibration Test.

For this task a daughterboard fully populated with the Beetle chips connected was used. The motherboard and the daughterboard were connected with ribbon cable and the system was powered. The test was carried out with Matlab for controlling the system.

The system could be calibrated correctly. Firstly, just the one ADC (ADC0 corresponding to Beetle 1) worked correctly. Secondly, both ADCs of the motherboard worked correctly during two or three days (figure 6 and figure 7). Finally the second ADC (ADC1 corresponding to Beetle 0) is not operational anymore and the measurements has been carried out with just the first ADC (ADC0 corresponding to Beetle 1).

The analogue readouts corresponding to different charges were measured and there is an agreement with the expected dynamic range of the Beetle chip. On the other hand, the analogue readout are as expected with a 16 bits header of 400 ns (figure 8) and 128 channels. During calibration, the amplitude of the channels are alternated. The first channel is negative, the second positive and so on (figure 9).

Finally, the digitized data is in agreement with the analogue readout and the noise level is below of 10 mV (figure 9, figure 10 and 11)

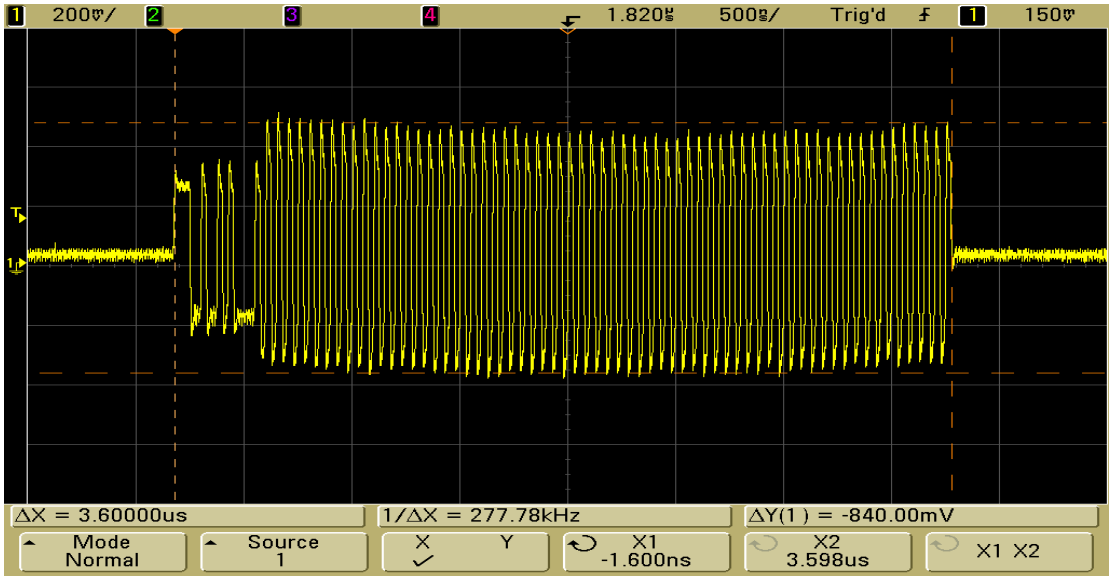

Figure 6. Analogue readout of Beetle 0 for a calibration charge corresponding to 51250 e-.

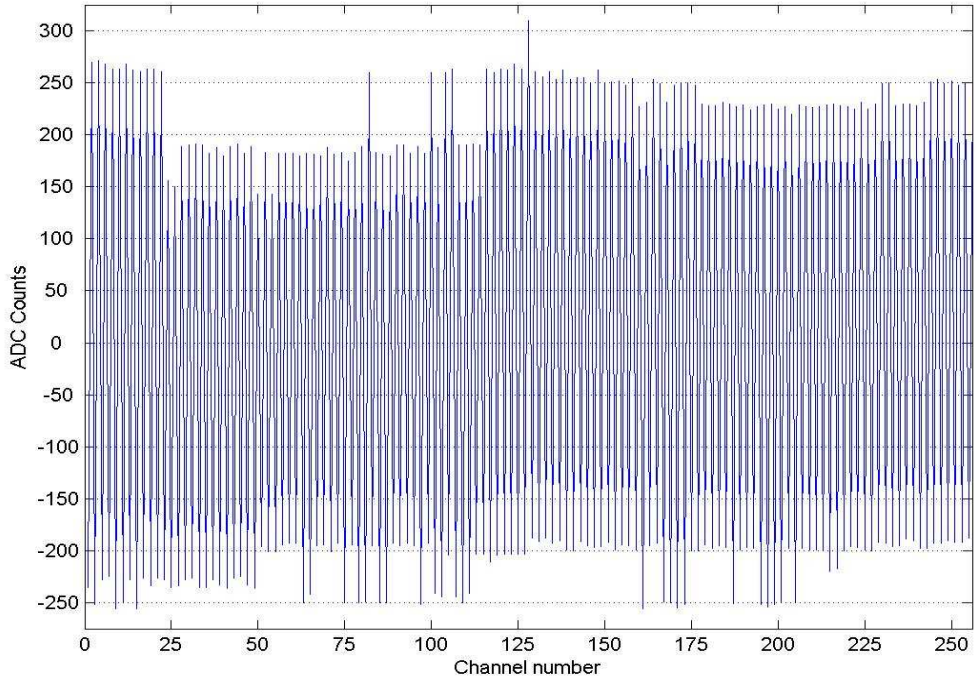

Figure 7. Digitized data corresponding to 51250 e- with both ADCs operational (channels 1 to 128 correspond to ADC0/Beetle 1 and channels 129 to 256 correspond to ADC1/Beetle 0; 1 ADC count = 2 mV).

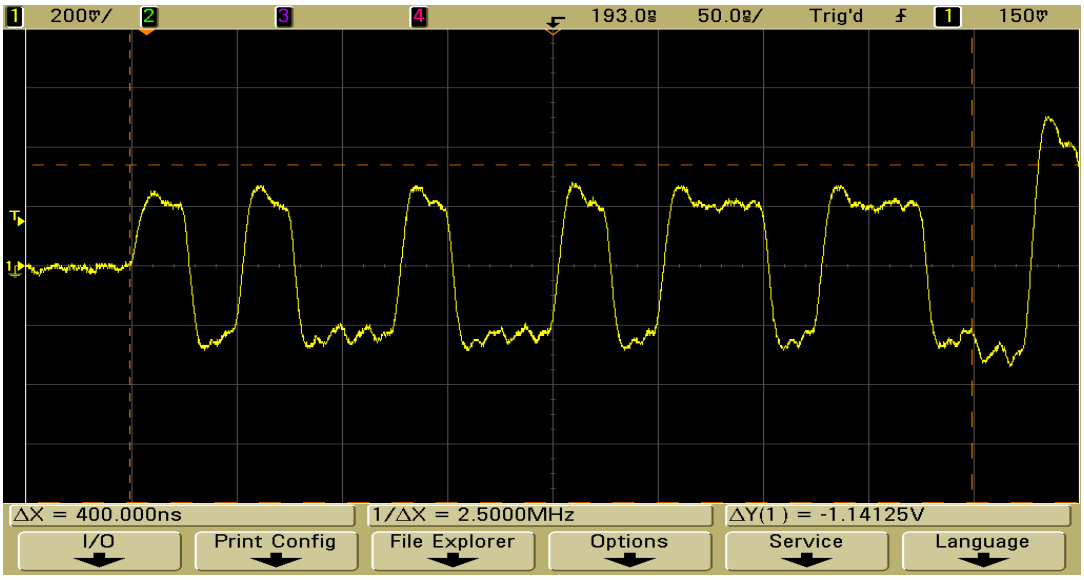

Figure 8. Header of an analogue readout of Beetle 1. Header of 16 bits corresponds to 400 ns (25 ns per bit).

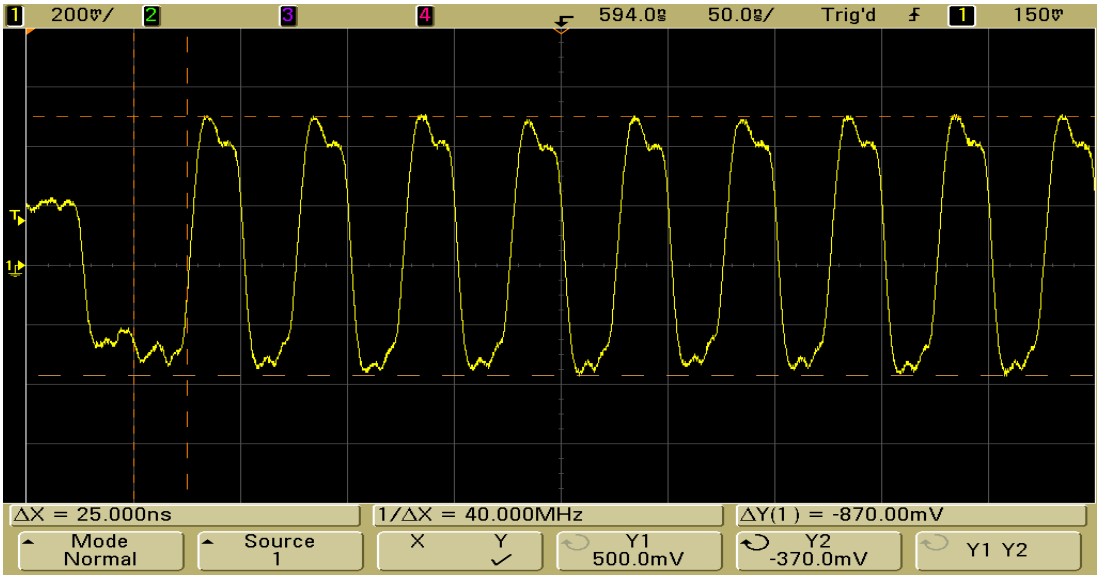

Figure 9. First channels of a calibration analogue readout of Beetle 1 corresponding to 51250 e-. The first channel is negative, the second positive and so on (25 ns per channel).

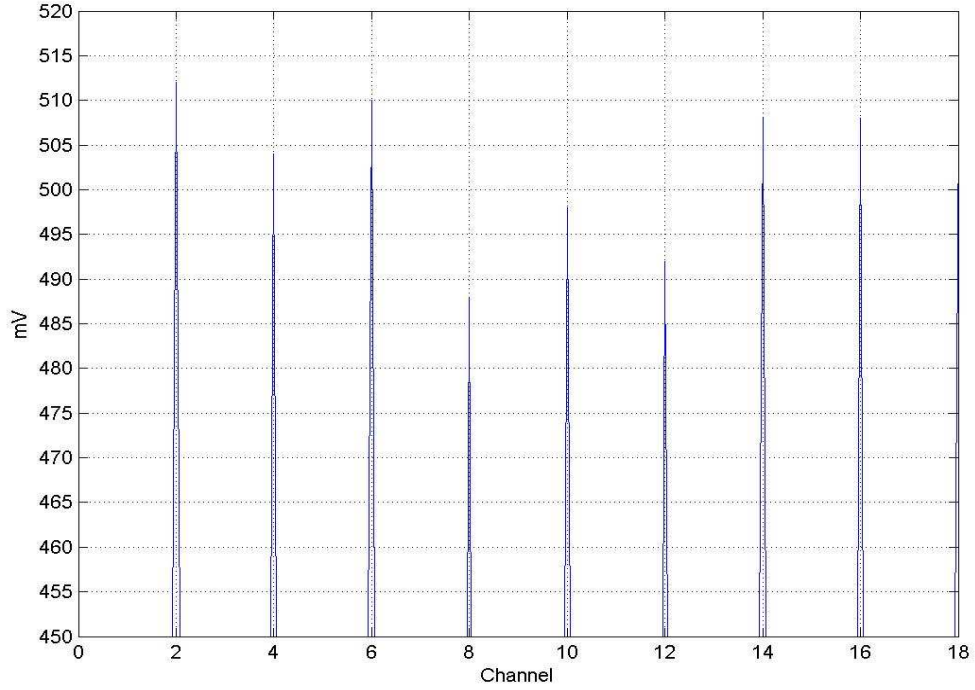

Figure 10. First digitized positive channels of a calibration analogue readout of Beetle 1 corresponding to 51250 e-.

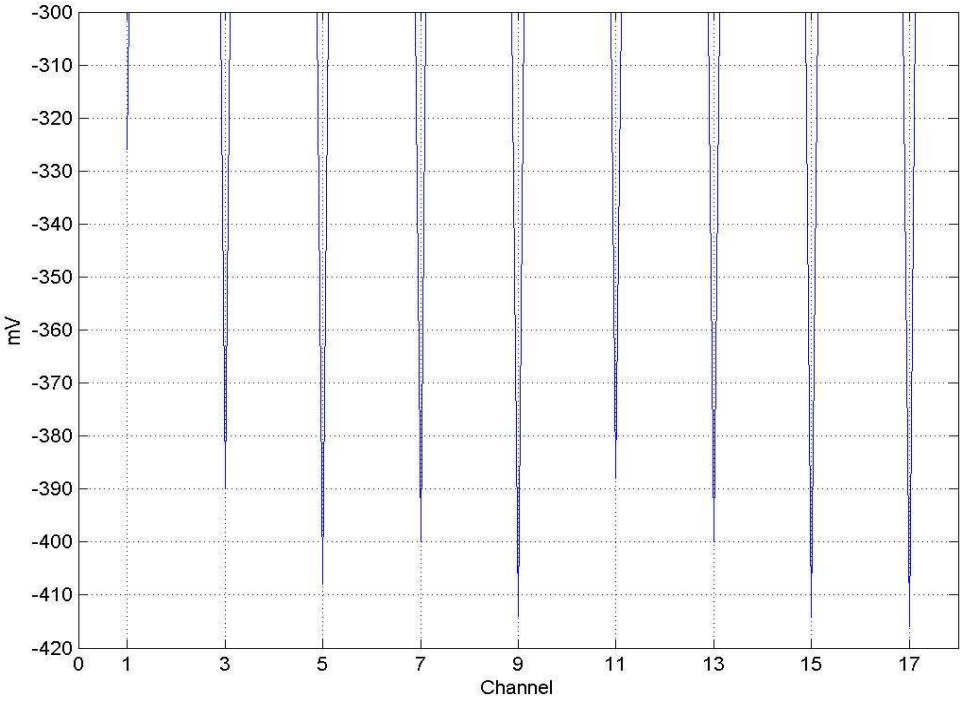

Figure 11. First digitized positive channels of a calibration analogue readout of Beetle 1 corresponding to 51250 e-.

5. Beetle Synchronization Test.

For this task a daughterboard fully populated with the Beetle chips connected was used. The motherboard and the daughterboard were connected with ribbon cable and the system was powered. The test was carried out with Matlab for controlling the system.

The system could be synchronized correctly. The TRIG_OUT pulse could be delayed in 1 ns steps (figure 12 and figure 13). Also, the internal laser trigger could be delayed in 25 ns steps (figure 14 and figure 15).

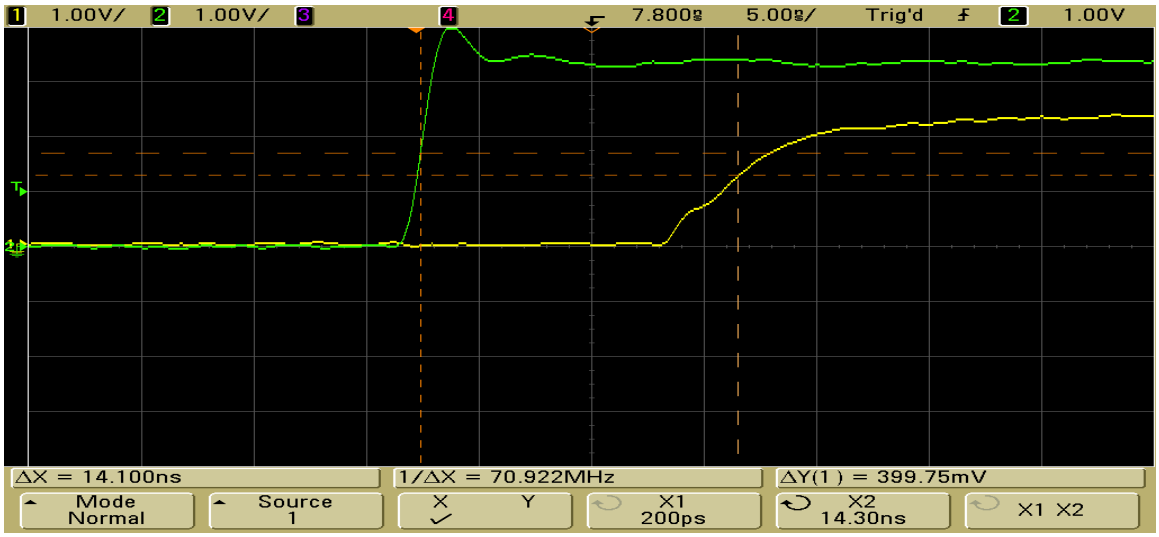

Figure 12. Trigger out signal before (green) and after (yellow) being delayed. This figure corresponds to a 0 ns delay on trigger out.

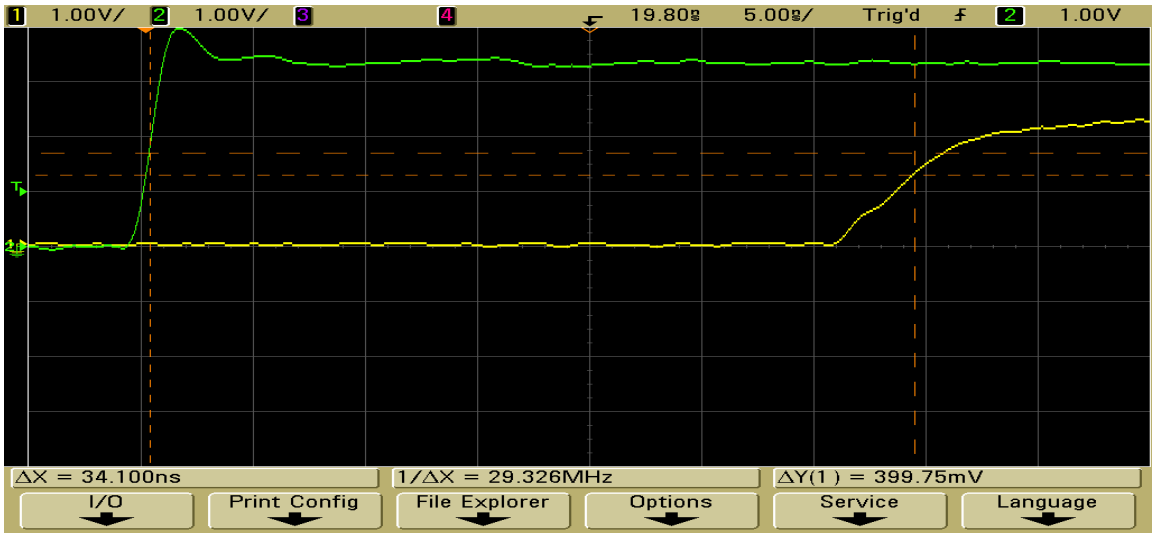

Figure 13. Trigger out signal before (green) and after (yellow) being delayed. This figure corresponds to a 20 ns delay on trigger out.

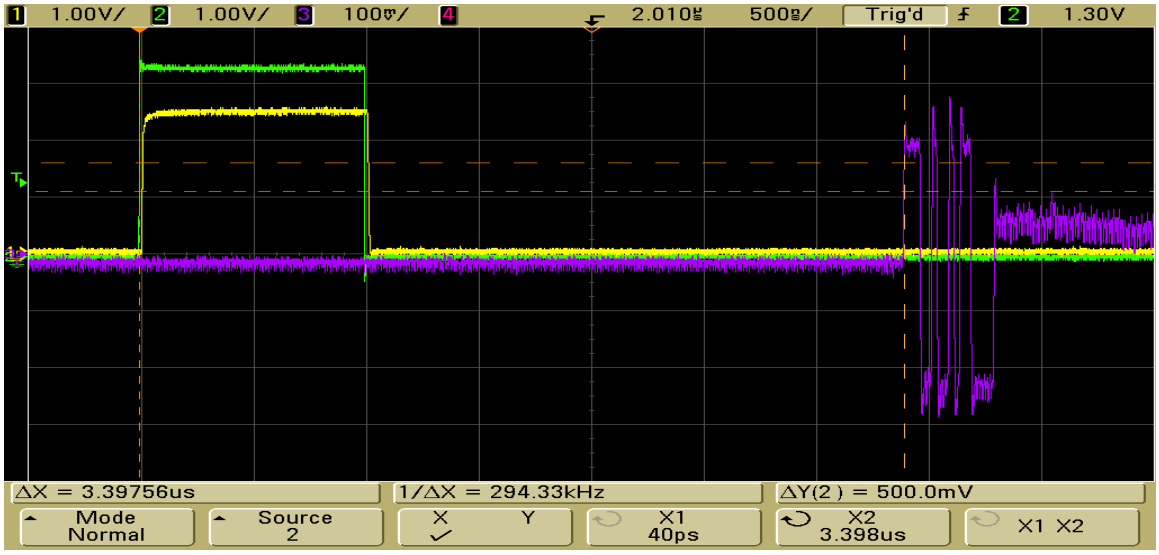

Figure 14. Trigger out signal before (green) and after (yellow) being delayed. Analogue readout (purple) for this trigger (no charge). This figure corresponds to a 0 ns delay on trigger out and 0 ns delay on Beetle trigger.

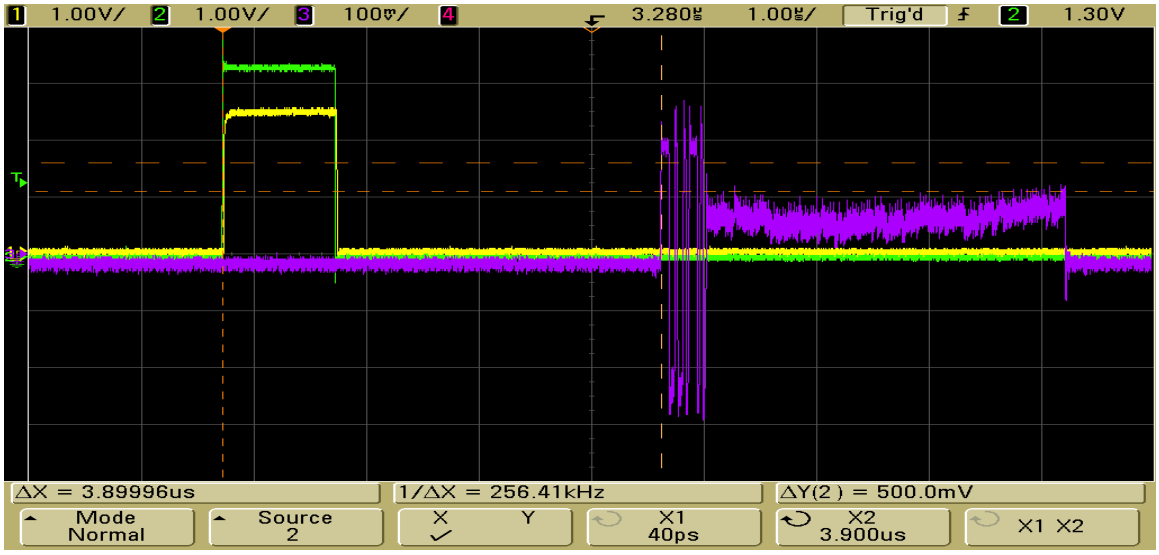

Figure 15. Trigger out signal before (green) and after (yellow) being delayed. Analogue readout (purple) for this trigger (no charge). This figure corresponds to a 0 ns delay on trigger out and 500 ns delay on Beetle trigger.

6. Laser acquisition and Laser Read test.

For this task a daughterboard fully populated with the Beetle chips connected was used. The motherboard and the daughterboard were connected with ribbon cable and the system was powered. The test was carried out with Matlab for controlling the system.

The system could acquire a laser acquisitions (without any charge) of different number of samples and then these samples could be read out by the software.

8. Conclusion.

The system is at the present time operational for Beetle configuration, calibration and for the laser setup. However, the ADC1 (corresponding to Beetle 0) is damaged and cannot be used. On the other hand, the system has been controlled using Matlab. The custom software developed by Carlos Lacasta has been tested only for Beetle configuration and calibration with good results. Therefore, we have to test the system with this software for Laser Synchronization, Laser Acquisition and Laser Read. The FPGA blocks corresponding to the radioactive source setup must be still developed (the DAC control and the TDC control) and tested. The corresponding hardware of these blocks is already designed and no changes are required for this hardware. We are going to order the production of 5 motherboards incorporating some minimal changes that are required.